IN THE CLAIMS:

Please amend claims 1, 12, 14, 20, and 32-34, so that a complete set of the pending claims will read as follows:

1. (currently amended) A method for accessing initialization data for starting up a central processor unit in a computer system comprising:

providing a non-volatile memory connected to a south-bridge chip, wherein the non-volatile memory includes a first memory space storing routines and code of a basic input/output system (BIOS) and a second memory space storing initialization data, and wherein the initialization data is excluded from the BIOS and is used for initialization of the central processor unit;

(a) starting up a north-bridge chip that is coupled between the central processor unit and [[a]] the south-bridge chip;

(b) sending a request from said north-bridge chip to the south-bridge chip in order to access the initialization data from the second memory space of [[a]] the non-volatile memory ~~which stores a basic input/output system (BIOS) and the initialization data~~;

(c) ~~upon receiving said initialization data from the south-bridge chip by said north-bridge chip,~~ starting up the central processor unit by receiving said initialization data from the south-bridge chip and then setting initial values for initialization of the central processor unit based on the received initialization data, wherein no random access memory is used to store said initialization data during step (c).

2. (previously presented) The method according to Claim 1 wherein said initialization data is serial initialization packet ("SIP") data of the central processor unit.

3. (previously presented) The method according to Claim 2 wherein said initialization data is SIP data for an AMD K7 processor.

4. (previously presented) The method according to Claim 1 wherein step (a) comprises starting up the north-bridge chip by said south-bridge chip.

5. (previously presented) The method according to Claim 1 wherein step (b) comprises sending a signal from said north bridge chip to said south-bridge chip for requesting said initialization data.

6. (previously presented) The method according to Claim 1 further comprising sending said initialization data from said north-bridge chip to the central processor unit of said computer system for starting up the central processor unit.

Claims 7-11 (cancelled).

12. (currently amended) A method for accessing initialization data for starting up a central processor unit in a computer system that also includes a bus, a south-bridge chip connected to the bus~~, a non-volatile memory~~, and a north-bridge chip connected between the bus and the central processor unit, the method comprising:

providing a non-volatile memory connected to the south-bridge chip, wherein the non-volatile memory includes a first memory space storing routines and code of a basic input/output system (BIOS) and a second memory space storing initialization data, and wherein the initialization data is excluded from the BIOS and is used for initialization of the central processor unit;

(a) sending a request from the north-bridge chip to the south-bridge chip in order to access the initialization data from the non-volatile memory~~, which stores a basic input/output system (BIOS) and the initialization data~~;

(b) in response to the request, accessing the second memory space of the non-volatile memory to read out the initialization data by the south-bridge chip;

(c) sending the initialization data from the south-bridge chip to the north-bridge chip; and

(d) ~~upon receiving the initialization data sent from the south-bridge chip,~~ activating the central processor unit by receiving the initialization data sent from the south-bridge chip and then setting initial values for initialization of the central processor unit based on the initialization data received by the north-bridge chip from the south-bridge chip, wherein no random access memory is used to store said initialization data during step (d).

13. (previously presented) The method of claim 12 further comprising activating the north-bridge chip by sending an initiating signal from the south-bridge chip to the north-bridge chip before step (a) is conducted.

14. (currently amended) The method of claim 13, further comprising activating the south bridge chip by a power supply before sending [[an]] the initiating signal from the south-bridge chip to actuate the north-bridge chip.

15. (previously presented) The method of claim 12 wherein the non-volatile memory is a read only memory.

16. (previously presented) The method of claim 12 wherein the request sent in step (a) is a transaction sent from the north-bridge chip to the south-bridge chip requesting the south-bridge chip to retrieve the initialization data from the non-volatile memory.

17. (previously presented) The method of claim 12 wherein step (d) includes:

receiving the initialization data by the north-bridge chip; and

sending an initializing signal and the received initialization data to the central processor unit.

18. (previously presented) The method of claim 17 wherein the initialization data includes an initialization ID.

19. (previously presented) The method of claim 17 wherein the initialization data includes serial initialization packet ("SIP") data.

20. (currently amended) A system for accessing initialization data for starting a central processor unit, the system comprising:

a non-volatile memory including: a first memory space storing routines and code of a basic input/output system (BIOS) and a second memory space storing the initialization data,

wherein the initialization data is excluded from the BIOS and is used for initialization of the central processor unit;

a south-bridge chip in direct communication with the non-volatile memory, the south-bridge chip, when requested for the initialization data, [[for]] accessing the initialization data from the second memory space of the non-volatile memory;

a north-bridge chip, coupled between the south-bridge chip and the central processor unit, the north-bridge chip, when activated, sending a request for the initialization data to the south-bridge chip;

wherein ~~upon receiving~~ in response to the request from the north-bridge chip for obtaining the initialization data, the south-bridge chip accesses the initialization data from the second memory space and forwards the initialization data to the north-bridge chip for activating the central processor unit;

wherein ~~upon receiving~~ in response to the initialization data sent from the south-bridge chip, the north-bridge chip ~~activates the central processor unit~~ sets initial values for initialization of the central processor unit based on the received initialization data from the south-bridge chip in order to activate the central processor unit without using any random access memory to store the initialization data.

21. (previously presented) The system of claim 20 further comprising a power supply for activating the south-bridge chip, wherein the south-bridge chip activates the north-bridge chip when the south-bridge chip is activated.

22. (previously presented) The system of claim 20 wherein the non-volatile memory is a read only memory.

23. (original) The system of claim 22 wherein the non-volatile memory includes a predetermined location for storing the initialization data that is not occupied by the BIOS.

24. (previously presented) The system of claim 20 wherein the initialization data includes an initialization ID.

25. (previously presented) The system of claim 20 wherein the initialization data includes session initialization protocol data.

26. (previously presented) The system of claim 20 wherein the south-bridge chip includes means for:

activating the north-bridge chip;

retrieving the initialization data by the south-bridge chip; and

sending the initialization data to the north-bridge chip.

27. (previously presented) The system of claim 20 where in the north-bridge chip further includes means for sending an initializing signal to the central processor unit based on the forwarded initialization data.

Claims 28-31 (cancelled).

32. (currently amended) The method of claim 1, wherein step (c) comprises:

~~upon~~ receiving said initialization data from the south-bridge chip by said north-bridge chip, and

~~starting up the central processor unit to~~ sending an initiating signal to the central processor unit to set the initial values for initialization of the central processor unit based on the received initialization data by said north-bridge chip, wherein no random access memory is used to store said initialization data during step (c).

33. (currently amended) The method of claim 12, wherein step (d) comprises:

~~upon~~ receiving the initialization data sent from the south-bridge chip by the north-bridge chip,

~~activating the central processor unit for to~~ sending an initiating signal to the central processor unit to set initial values for initialization of the central processor unit based on the received initialization data received by the north-bridge chip from the south-bridge chip, wherein no random access memory is used to store said initialization data during step (d).

34. (currently amended) The apparatus according to claim 20, wherein ~~upon receiving~~ in response to the initialization data sent from the south-bridge chip, the north-bridge chip ~~activates the central processor unit~~ sends an initiating signal to the central processor unit to set the initial values for initialization of the central processor unit based on the received initialization data from the south-bridge chip in order to activate the central processor unit without using any random access memory to store the initialization data.